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DATE: Thursday, August 19, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L3	((treatment chamber) or CVD or (process chamber)) and (carboxylic acid) and (removing metal)	37
		DB=USPT; PLUR=YES; OP=ADJ	
☐	L2	5993679.pn.	1
☐	L1	5413758.pn.	1

END OF SEARCH HISTORY

h e b b cg b chh e c f c e e

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 10 of 37 returned.

☐ 1. Document ID: US 20040091820 A1

L3: Entry 1 of 37 File: PGPB May 13, 2004

PGPUB-DOCUMENT-NUMBER: 20040091820
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040091820 A1

TITLE: Method for removing resist pattern and method for manufacturing semiconductor device

PUBLICATION-DATE: May 13, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nagai, Masaharu	Kanagawa		JP	
Ogino, Kiyofumi	Kanagawa		JP	
Nakai, Teruhisa	Tochigi		JP	
Shioda, Eiji	Tochigi		JP	

US-CL-CURRENT: 430/317; 430/165, 430/313, 430/326, 430/329

ABSTRACT:

It is an object to provide a technique for removing a resist favorably without leaving residue in the case of using a nonaqueous resist stripper. According to the present invention, in order to achieve the object, when a resist pattern is removed by using the nonaqueous resist stripper, it becomes easier to remove the resist pattern after dry etching or ion doping, by performing exposure treatment on the resist pattern. After a resist pattern is formed from a DNQ-novolac resin type of positive resist composition, the resist pattern is irradiated with light within the range of photosensitive wavelength of the DNQ photosensitizer, thereby removing the resist pattern with the nonaqueous resist stripper.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20040038529 A1

L3: Entry 2 of 37 File: PGPB Feb 26, 2004

PGPUB-DOCUMENT-NUMBER: 20040038529
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040038529 A1

h e b b g e e e f e c e e e

TITLE: Process for producing integrated circuits

PUBLICATION-DATE: February 26, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Soininen, Pekka Juha	Espoo	OR	FI	
Elers, Kai-Erik	Portland		US	

US-CL-CURRENT: 438/685; 257/E21.171, 257/E21.241, 257/E21.576, 257/E21.582, 257/E21.584, 257/E21.591, 438/686, 438/687, 438/785

ABSTRACT:

This invention concerns a process for producing integrated circuits containing at least one layer of elemental metal which during the processing of the integrated circuit is at least partly in the form of metal oxide, and the use of an organic compound containing certain functional groups for the reduction of a metal oxide layer formed during the production of an integrated circuit. According to the present process the metal oxide layer is at least partly reduced to elemental metal with a reducing agent selected from organic compounds containing one or more of the following functional groups: alcohol (--OH), aldehyde (--CHO), and carboxylic acid (--COOH).

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 20040002430 A1

L3: Entry 3 of 37 File: PGPB Jan 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040002430
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040002430 A1

TITLE: Using a time critical wafer cleaning solution by combining a chelating agent with an oxidizer at point-of-use

PUBLICATION-DATE: January 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Verhaverbeke, Steven	San Francisco	CA	US	

US-CL-CURRENT: 510/175; 134/100.1, 134/153, 134/3, 134/33, 134/36, 134/902, 257/E21.228

ABSTRACT:

A wafer cleaning solution that includes a solution of NH4OH, a carboxylic acid based chelating agent, H2O, and an oxidizer.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

4. Document ID: US 20030162399 A1

L3: Entry 4 of 37 File: PGPB Aug 28, 2003

PGPUB-DOCUMENT-NUMBER: 20030162399
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030162399 A1

TITLE: Method, composition and apparatus for tunable selectivity during chemical mechanical polishing of metallic structures

PUBLICATION-DATE: August 28, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Singh, Rajiv K.	Gainesville	FL	US	

US-CL-CURRENT: 438/692; 257/E21.304

ABSTRACT:

A slurry and method for chemical mechanical polishing (CMP) a structure including at least one metal based film and at least one underlying dielectric film includes at least one selective adsorption additive, such as a surfactant or a polymer. The metal film does not substantially adsorb the selective adsorption additive surfactant, while dielectric film substantially adsorbs the selective adsorption additive. A plurality of composite particles can be added, such as inorganic cores surrounded by the selective adsorption additive. In another embodiment, a slurry and method for polishing a metal film and an underlying dielectric film includes polishing during a first time interval using a first slurry composition and polishing during a second time interval with a second slurry composition, wherein a selectivity ratio for metal/dielectric polishing using the first slurry composition to the metal/dielectric selectivity using the second slurry composition is at least 1.3.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

5. Document ID: US 20030153183 A1

L3: Entry 5 of 37 File: PGPB Aug 14, 2003

PGPUB-DOCUMENT-NUMBER: 20030153183
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030153183 A1

TITLE: Process for chemical mechanical polishing of semiconductor substrate and aqueous dispersion for chemical mechanical polishing

PUBLICATION-DATE: August 14, 2003

h e b b g e e e f e c e e e

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Konno, Tomohisa	Tokyo		JP	
Motonari, Masayuki	Tokyo		JP	
Hattori, Masayuki	Tokyo		JP	
Kawahashi, Nobuo	Tokyo		JP	

US-CL-CURRENT: 438/689; 257/E21.304

ABSTRACT:

The object of the present invention is to provide a process for chemical mechanical polishing of semiconductor substrate that is particularly useful for chemical mechanical polishing a wafer having a wiring pattern and an insulating layer having a low dielectric constant is formed between wiring patterns, interlayers in the case of a multi-layer wiring and the like in the process of producing a semiconductor device, and an aqueous dispersion for chemical mechanical polishing which is used in this process. The process for chemical mechanical polishing of a semiconductor substrate of the present invention is that a surface to be polished of the semiconductor substrate is polished under conditions of a rotation speed of a polishing table fixing a polishing pad at the range from 50 to 200 rpm and a pressing pressure of the semiconductor substrate fixed to a polishing head against a polishing pad at the range from 700 to 18,000 Pa, by using an aqueous dispersion for chemical mechanical polishing comprising an abrasive and at least one compound selected from the group consisting of polycarboxylic acid having a heterocycle and anhydride thereof, and the polishing pad.

☐ 6. Document ID: US 20030087524 A1

L3: Entry 6 of 37 File: PGPB May 8, 2003

PGPUB-DOCUMENT-NUMBER: 20030087524
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030087524 A1

TITLE: Cleaning method, method for fabricating semiconductor device and cleaning solution

PUBLICATION-DATE: May 8, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Aoki, Hidemitsu	Tokyo		JP	
Tomimori, Hiroaki	Tokyo		JP	
Yamamoto, Kenichi	Tokyo		JP	

US-CL-CURRENT: 438/691; 257/E21.252, 257/E21.304, 438/692, 438/693, 438/734

ABSTRACT:

h e b b g e e e f e c e e e

A cleaning solution having an oxidation-reduction potential lower than that of pure water and a pH value of 4 or below is used to remove metal contamination, thereby efficiently removing the metal contamination adhered onto a surface of a substrate without damaging an underlayer.

7. Document ID: US 20030082296 A1

L3: Entry 7 of 37 File: PGPB May 1, 2003

PGPUB-DOCUMENT-NUMBER: 20030082296
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030082296 A1

TITLE: Metal nitride deposition by ALD with reduction pulse

PUBLICATION-DATE: May 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Elers, Kai	Helsinki		FI	
Li, Wei-Min	Espoo		FI	

US-CL-CURRENT: 427/96; 257/E21.168, 427/255.28, 427/255.39

ABSTRACT:

The present methods provide tools for growing conformal metal thin films, including metal nitride, metal carbide and metal nitride carbide thin films. In particular, methods are provided for growing such films from aggressive chemicals. The amount of corrosive chemical compounds, such as hydrogen halides, is reduced during the deposition of transition metal, transition metal carbide, transition metal nitride and transition metal nitride carbide thin films on various surfaces, such as metals and oxides. Getter compounds protect surfaces sensitive to hydrogen halides and ammonium halides, such as aluminum, copper, silicon oxide and the layers being deposited, against corrosion. Nanolaminate structures incorporating metallic thin films, and methods for forming the same, are also disclosed.

8. Document ID: US 20020108861 A1

L3: Entry 8 of 37 File: PGPB Aug 15, 2002

PGPUB-DOCUMENT-NUMBER: 20020108861
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020108861 A1

TITLE: Method and apparatus for electrochemical planarization of a workpiece

h e b b g e e e f e c e e e

PUBLICATION-DATE: August 15, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Emesh, Ismail	Gilbert	AZ	US	
Chadda, Saket	Chandler	AZ	US	
Korovin, Nikolay	Phoenix	AZ	US	
Mueller, Brian L.	Chandler	AZ	US	

US-CL-CURRENT: 205/81; 204/212, 204/222, 204/224M, 204/229.4, 204/229.8, 205/108, 205/124, 205/645, 205/653, 205/656, 205/663

ABSTRACT:

An electrochemical planarization apparatus for planarizing a metallized surface on a workpiece includes a polishing pad and a platen. The platen is formed of conductive material, is disposed proximate to the polishing pad and is configured to have a negative charge during at least a portion of a planarization process. At least one electrical conductor is positioned within the platen. The electrical conductor has a first end connected to a power source. A workpiece carrier is configured to carry a workpiece and press the workpiece against the polishing pad. The power source applies a positive charge to the workpiece via the electrical conductor so that an electric potential difference between the metallized surface of the workpiece and the platen is created to remove at least a portion of the metallized surface from the workpiece.

☐ 9. Document ID: US 20020102852 A1

L3: Entry 9 of 37 File: PGPB Aug 1, 2002

PGPUB-DOCUMENT-NUMBER: 20020102852
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020102852 A1

TITLE: Cleaning method and solution for cleaning a wafer in a single wafer process

PUBLICATION-DATE: August 1, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Verhaverbeke, Steven	San Francisco	CA	US	
Truman, J. Kelly	Morgan Hill	CA	US	

US-CL-CURRENT: 438/690; 257/E21.228

ABSTRACT:

The present invention is a novel cleaning method and a solution for use in a single wafer cleaning process. According to the present invention the cleaning solution comprises ammonium hydroxide (NH.sub.4OH), hydrogen peroxide (H.sub.2O.sub.2),

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water (H.sub.2O) and a chelating agent. In an embodiment of the present invention the cleaning solution also contains a surfactant. And still yet another embodiment of the present invention the cleaning solution also comprises a dissolved gas such as H.sub.2. In a particular embodiment of the present invention, this solution is used by spraying or dispensing it on a spinning wafer.

☐ 10. Document ID: US 20020034874 A1

L3: Entry 10 of 37 File: PGPB Mar 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020034874
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020034874 A1

TITLE: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

PUBLICATION-DATE: March 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
AOKI, HIDEMITSU	TOKYO		JP	

US-CL-CURRENT: 438/689; 257/E21.577, 257/E21.579

ABSTRACT:

In a method of manufacturing a semiconductor device having a multi-layer interconnection, after a via hole has been formed, the inside of the via hole is cleaned using a cleaning solution containing a complexing agent capable of forming a complex with contaminants of copper type metals.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Term	Documents
TREATMENT	1812453
TREATMENTS	209574
CHAMBER	1848118
CHAMBERS	517795
CVD	121465
CVDS	77
PROCESS	4742195

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PROCESSES	1353030
CARBOXYLIC	416318
CARBOXYLICS	82
ACID	2257030
(((TREATMENT CHAMBER) OR CVD OR (PROCESS CHAMBER)) AND (CARBOXYLIC ACID) AND (REMOVING METAL)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	37

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Previous Page Next Page Go to Doc#

h e b b g e e e f e c e e e

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Search Results - Record(s) 11 through 20 of 37 returned.

☐ 11. Document ID: US 20020031985 A1

L3: Entry 11 of 37 File: PGPB Mar 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020031985
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020031985 A1

TITLE: Chemical mechanical polishing composition and process

PUBLICATION-DATE: March 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wang, Yuchun	San Jose	CA	US	
Bajaj, Rajeev	Fremont	CA	US	
Redeker, Fred C.	Fremont	CA	US	
Li, Shijian	San Jose	CA	US	

US-CL-CURRENT: 451/41

ABSTRACT:

A method and composition for planarizing a substrate surface is provided. The polishing composition includes an oxidizer capable of oxidizing a metal undergoing planarization and yielding a complexing agent which complexes with the oxidized metal and a stabilizer such as a stannate salt. The composition may further include abrasive particles and/or inhibitors. The composition may be used in a multi-step polishing process including polishing a substrate surface to selectively remove a metal layer with respect to a barrier layer and dielectric layer and polishing a substrate surface using the composition to non-selectively remove the metal layer, a barrier layer, and a dielectric layer from the substrate surface.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 12. Document ID: US 20020028585 A1

L3: Entry 12 of 37 File: PGPB Mar 7, 2002

PGPUB-DOCUMENT-NUMBER: 20020028585
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020028585 A1

h e b b cg b cc e

TITLE: Method of removing contaminants from integrated circuit substrates using cleaning solutions

PUBLICATION-DATE: March 7, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chung, Seung-Pil	Seoul		KR	
Chang, Kyu-Hwan	Hwasung-gun		KR	
Kwon, Young-Min	Suwon-city		KR	
Hah, Sang-Lock	Seoul		KR	

US-CL-CURRENT: 438/765; 134/1.2, 257/E21.226, 257/E21.228, 257/E21.229, 438/795

ABSTRACT:

A method for removing contaminants from an integrated circuit substrate include treating the substrate with a hydrogen peroxide cleaning solution containing a chelating agent, and treating the substrate with hydrogen gas and fluorine-containing gas, and annealing the substrate. Cleaning solutions includes ammonium, hydrogen peroxide, deionized water, and chelating agent. The chelating agent includes one to three compounds selected from the group consisting of carboxylic acid compounds, phosphonic acid compounds, and hydroxyl aromatic compounds. The fluorine-containing gas is a gas selected from the group consisting of nitrogen trifluoride (NF3), hexafluorosulphur (SF.sub.6), and trifluorochlorine (ClF.sub.3).

13. Document ID: US 20010030367 A1

L3: Entry 13 of 37 File: PGPB Oct 18, 2001

PGPUB-DOCUMENT-NUMBER: 20010030367
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010030367 A1

TITLE: Semiconductor integrated circuit device and fabrication method for semiconductor integrated circuit device

PUBLICATION-DATE: October 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Noguchi, Junji	Ome		JP	
Ohashi, Naohumi	Hannou		JP	
Saito, Tatsuyuki	Ome		JP	

US-CL-CURRENT: 257/758; 257/E21.576, 257/E21.577, 257/E21.579, 257/E21.582, 438/622

ABSTRACT:

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Cu interconnections embedded in an interconnection slot of a silicon oxide film are formed by polishing using CMP to improve the insulation breakdown resistance of a copper interconnection formed using the Damascene method, and after a post-CMP cleaning step, the surface of the silicon oxide film and Cu interconnections is treated by a reducing plasma (ammonia plasma). Subsequently, a continuous cap film (silicon nitride film) is formed without vacuum break.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 14. Document ID: US 20010029104 A1

L3: Entry 14 of 37 File: PGPB Oct 11, 2001

PGPUB-DOCUMENT-NUMBER: 20010029104
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010029104 A1

TITLE: Substrate-cleaning method and substrate-cleaning solution

PUBLICATION-DATE: October 11, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Aoki, Hidemitsu	Tokyo		JP	

US-CL-CURRENT: 438/692; 257/E21.228

ABSTRACT:

In cleaning a substrate which has a metal material and a semiconductor material both exposed at the surface and which has been subjected to a chemical mechanical polishing treatment, the substrate is first cleaned with a first cleaning solution containing ammonia water, etc. and then with a second cleaning solution containing (a) a first complexing agent capable of easily forming a complex with the oxide of said metal material, etc. and (b) an anionic or cationic surfactant.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 15. Document ID: US 20010020478 A1

L3: Entry 15 of 37 File: PGPB Sep 13, 2001

PGPUB-DOCUMENT-NUMBER: 20010020478
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010020478 A1

TITLE: Cleaning method of tratment equipment and treatment equipment

PUBLICATION-DATE: September 13, 2001

h e b b cg b cc e

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kojima, Yasuhiko	Nirasaki-shi		JP	
Oshima, Yasuhiro	Nirasaki-shi		JP	

US-CL-CURRENT: 134/3; 134/102.1, 134/21, 134/36, 134/37

ABSTRACT:

In a state of the inside of a treatment chamber of treatment equipment being evacuated, therein a cleaning gas containing trifluoroaceticacid (TFA) as a cleaning agent is supplied. Metal such as copper used in the formation of an interconnection or an electrode and stuck on an inner wall surface of the treatment chamber, when coming into contact with the cleaning agent (TFA) in the cleaning gas, without forming an oxide or a metallic salt, is directly complexed. The complex is sublimed due to the evacuation and is exhausted outside the treatment chamber. Accordingly, at less labor and low cost, the cleaning can be efficiently implemented.

☐ 16. Document ID: US 6774041 B1

L3: Entry 16 of 37 File: USPT Aug 10, 2004

US-PAT-NO: 6774041
DOCUMENT-IDENTIFIER: US 6774041 B1

TITLE: Polishing method, metallization fabrication method, method for manufacturing semiconductor device and semiconductor device

DATE-ISSUED: August 10, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kondo; Seiichi	Kokubunji			JP
Fujimori; Masaaki	Hatoyama			JP
Sakuma; Noriyuki	Hachioji			JP
Homma; Yoshio	Hinode			JP

US-CL-CURRENT: 438/692; 216/101, 216/103, 216/105, 216/88, 216/91, 438/714

ABSTRACT:

Described is a polishing technique adapted for multilevel metallization of an electronic circuit device, which comprises polishing a metal film with a polishing liquid containing an oxidizing substance, a phosphoric acid and a protection-layer forming agent. The present invention makes it possible to polishing a metal film at a high removal rate while suppressing occurrence of scratches, delamination, dishing or erosion.

21 Claims, 26 Drawing figures

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Exemplary Claim Number: 1
Number of Drawing Sheets: 11

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

17. Document ID: US 6770483 B2

L3: Entry 17 of 37 File: USPT Aug 3, 2004

US-PAT-NO: 6770483
DOCUMENT-IDENTIFIER: US 6770483 B2

TITLE: Determination of multi-valent metal contamination and system for removal of multi-valent metal contaminants from water

DATE-ISSUED: August 3, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lyon; Irving	Los Angeles	CA	90034	

US-CL-CURRENT: 436/39; 210/719, 210/94, 436/41, 436/73, 436/83, 436/84

ABSTRACT:

A test for determining the presence of multi-valent metal contaminants, such as arsenic, mercury and chromium, when present in certain valence states and a system for removal of these contaminants from water. Multi-valent metal salts, for example, Cr.sup.+6, which are highly toxic, can be detected and potentially removed from water through a redox reaction by reaction with iron or cobalt salts to obtain a reductive elimination of the Cr.sup.+6 by conversion to Cr.sup.+3. The determination may be in the form of a test, such that a tableted composition can be introduced into water for reduction of a metal salt, such as Cr.sup.+6 to Cr.sup.+3 in order to provide a visual indication thereof. The system for the conversion of Cr.sup.+6 or other reducible metal salts to other lower valence states having less toxicity would rely upon introduction of a metal salt in the form of a reducing agent which would be introduced into the water allowing for a reduction/oxidation action to take place. This would be followed by removal of the flocculated/precipitated reduced contaminant metal salt and by re-reduction of the oxidized reducing agent.

43 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

18. Document ID: US 6764950 B2

L3: Entry 18 of 37 File: USPT Jul 20, 2004

h e b b cg b cc e

US-PAT-NO: 6764950
DOCUMENT-IDENTIFIER: US 6764950 B2

TITLE: Fabrication method for semiconductor integrated circuit device

DATE-ISSUED: July 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Noguchi; Junji	Ome			JP
Ohashi; Naohumi	Hannou			JP
Saito; Tatsuyuki	Ome			JP

US-CL-CURRENT: 438/687; 438/626, 438/627, 438/631, 438/643, 438/645

ABSTRACT:

Cu interconnections embedded in an interconnection slot of a silicon oxide film are formed by polishing using CMP to improve the insulation breakdown resistance of a copper interconnection formed using the Damascene method, and after a post-CMP cleaning step, the surface of the silicon oxide film and Cu interconnections is treated by a reducing plasma (ammonia plasma). Subsequently, a continuous cap film (silicon nitride film) is formed without vacuum break.

12 Claims, 145 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 78

☐ 19. Document ID: US 6736952 B2

L3: Entry 19 of 37 File: USPT May 18, 2004

US-PAT-NO: 6736952
DOCUMENT-IDENTIFIER: US 6736952 B2

TITLE: Method and apparatus for electrochemical planarization of a workpiece

DATE-ISSUED: May 18, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Emesh; Ismail	Gilbert	AZ		
Chadda; Saket	Chandler	AZ		
Korovin; Nikolay N.	Phoenix	AZ		
Mueller; Brian L.	Chandler	AZ		

US-CL-CURRENT: 205/81; 204/212, 204/217, 204/224M, 204/228.7, 205/108, 205/123, 205/124, 205/222, 205/223, 205/641, 205/663, 205/93, 451/287, 451/288, 451/36

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ABSTRACT:

An electrochemical planarization apparatus for planarizing a metallized surface on a workpiece includes a polishing pad and a platen. The platen is formed of conductive material, is disposed proximate to the polishing pad and is configured to have a negative charge during at least a portion of a planarization process. At least one electrical conductor is positioned within the platen. The electrical conductor has a first end connected to a power source. A workpiece carrier is configured to carry a workpiece and press the workpiece against the polishing pad. The power source applies a positive charge to the workpiece via the electrical conductor so that an electric potential difference between the metallized surface of the workpiece and the platen is created to remove at least a portion of the metallized surface from the workpiece.

74 Claims, 11 Drawing figures
Exemplary Claim Number: 37
Number of Drawing Sheets: 8

☐ 20. Document ID: US 6596638 B1

L3: Entry 20 of 37 File: USPT Jul 22, 2003

US-PAT-NO: 6596638
DOCUMENT-IDENTIFIER: US 6596638 B1

TITLE: Polishing method

DATE-ISSUED: July 22, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kondo; Seiichi	Kokubunji			JP
Homma; Yoshio	Tokyo			JP
Sakuma; Noriyuki	Hachiouji			JP
Takeda; Kenichi	Tokorozawa			JP
Hinode; Kenji	Hachiouji			JP

US-CL-CURRENT: 438/690; 257/E21.304, 438/691, 438/692, 438/693, 438/700

ABSTRACT:

A polishing technique wherein scratches, peeling, dishing and erosion are suppressed, a complex cleaning process and slurry supply/processing equipment are not required, and the cost of consumable items, such as slurries and polishing pads, is reduced. A metal film formed on an insulating film having a groove is polished with a polishing solution containing an oxidizer and a substance which renders oxides water-soluble, but not containing a polishing abrasive.

41 Claims, 41 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 26

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Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Term	Documents
TREATMENT	1812453
TREATMENTS	209574
CHAMBER	1848118
CHAMBERS	517795
CVD	121465
CVDS	77
PROCESS	4742195
PROCESSES	1353030
CARBOXYLIC	416318
CARBOXYLICS	82
ACID	2257030
(((TREATMENT CHAMBER) OR CVD OR (PROCESS CHAMBER)) AND (CARBOXYLIC ACID) AND (REMOVING METAL)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	37

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Display Format: REV Change Format

Previous Page Next Page Go to Doc#

h e b b cg b cc e

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 21 through 30 of 37 returned.

☐ 21. Document ID: US 6566276 B2

L3: Entry 21 of 37 File: USPT May 20, 2003

US-PAT-NO: 6566276
DOCUMENT-IDENTIFIER: US 6566276 B2

TITLE: Method of making electronic materials

DATE-ISSUED: May 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maloney; David J.	Pleasanton	CA		
Lee; Wai M.	Fremont	CA		
Roman, Jr.; Paul J.	Pleasanton	CA		
Fury; Michael A.	San Francisco	CA		
Hill; Ross H.	Coquitlam			CA

US-CL-CURRENT: 438/758; 430/311, 430/312

ABSTRACT:

The present invention involves fabrication of a hard mask. An embodiment involves the conversion of a precursor into a top-surface imaging layer during a direct patterning step. Another embodiment of the present invention is a method of forming an etched pattern in a substrate. A further embodiment of the present invention is a method of forming an implanted region in a substrate. Preferred precursors are formed from a metal complex comprising at least one ligand selected from the group consisting of acac, carboxylato, alkoxy, azide, carbonyl, nitrato, amine, halide, nitro, and mixtures thereof and at least one metal selected from the group consisting of Li, Al, Si, Ti, V, Cr, Mn, Fe, Ni, Co, Cu, Zn, Sr, Y, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Sn, Ba, La, Pr, Sm, Eu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Pb, Th, U, Sb, As, Ce, Mg, and mixtures thereof.

46 Claims, 100 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 30

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 22. Document ID: US 6513538 B2

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L3: Entry 22 of 37 File: USPT Feb 4, 2003

US-PAT-NO: 6513538
DOCUMENT-IDENTIFIER: US 6513538 B2

TITLE: Method of removing contaminants from integrated circuit substrates using cleaning solutions

DATE-ISSUED: February 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chung; Seung-pil	Seoul			KR
Chang; Kyu-hwan	Kyungki-do			KR
Kwon; Young-min	Suwon			KR
Hah; Sang-lock	Seoul			KR

US-CL-CURRENT: 134/1.2; 134/26, 134/30, 134/36, 134/902, 216/63, 216/67, 216/74, 257/E21.226, 257/E21.228, 257/E21.229, 438/704, 438/715, 438/746, 438/906

ABSTRACT:

A method for removing contaminants from an integrated circuit substrate include treating the substrate with a hydrogen peroxide cleaning solution containing a chelating agent, and treating the substrate with hydrogen gas and fluorine-containing gas, and annealing the substrate. Cleaning solutions includes ammonium, hydrogen peroxide, deionized water, and chelating agent. The chelating agent includes one to three compounds selected from the group consisting of carboxylic acid compounds, phosphonic acid compounds, and hydroxyl aromatic compounds. The fluorine-containing gas is a gas selected from the group consisting of nitrogen trifluoride (NF3), hexafluorosulphur (SF.sub.6), and trifluorochlorine (ClF.sub.3).

20 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

☐ 23. Document ID: US 6509273 B1

L3: Entry 23 of 37 File: USPT Jan 21, 2003

US-PAT-NO: 6509273
DOCUMENT-IDENTIFIER: US 6509273 B1

TITLE: Method for manufacturing a semiconductor device

DATE-ISSUED: January 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Imai; Toshinori	Ome			JP

h e b b cg b cc e

Ohashi; Naofumi	Hanno	JP
Homma; Yoshio	Hinode	JP
Kondo; Seiichi	Kokubunji	JP

US-CL-CURRENT: 438/693; 257/E21.304, 438/691

ABSTRACT:

Problematic dishing and erosion in forming embedded metal interconnection by a chemical mechanical polishing (CMP) method are suppressed.

Formation of embedded Cu interconnects 46a to 46e by chemical mechanical polishing of a Cu film 46 formed in interconnect trenches 40 to 44 is performed by abrasive-grain-free chemical mechanical polishing using a polishing liquid of an abrasive grain content less than 0.5 wt % (CMP of the first step); with-abrasive-grain chemical mechanical polishing using a polishing liquid of an abrasive grain content of 0.5 or more wt % (CMP of the second step); and selective chemical mechanical polishing using a polishing liquid to which an anticorrosive such as benzotriazole (BTA) is added (CMP of the third step).

45 Claims, 31 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 25

24. Document ID: US 6444583 B2

L3: Entry 24 of 37 File: USPT Sep 3, 2002

US-PAT-NO: 6444583
DOCUMENT-IDENTIFIER: US 6444583 B2

TITLE: Substrate-cleaning method and substrate-cleaning solution

DATE-ISSUED: September 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aoki; Hidemitsu	Tokyo			JP

US-CL-CURRENT: 438/692; 257/E21.228, 438/252, 510/175

ABSTRACT:

In cleaning a substrate which has a metal material and a semiconductor material both exposed at the surface and which has been subjected to a chemical mechanical polishing treatment, the substrate is first cleaned with a first cleaning solution containing ammonia water, etc. and then with a second cleaning solution containing (a) a first complexing agent capable of easily forming a complex with the oxide of said metal material, etc. and (b) an anionic or cationic surfactant.

15 Claims, 9 Drawing figures

h e b b cg b cc e

Exemplary Claim Number: 1
Number of Drawing Sheets: 9

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

25. Document ID: US 6423148 B1

L3: Entry 25 of 37 File: USPT Jul 23, 2002

US-PAT-NO: 6423148
DOCUMENT-IDENTIFIER: US 6423148 B1

TITLE: Substrate-cleaning method and substrate-cleaning solution

DATE-ISSUED: July 23, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aoki; Hidemitsu	Tokyo			JP

US-CL-CURRENT: 134/3; 134/28, 134/29, 134/41, 134/902, 216/38, 216/88, 257/E21.228, 438/692, 438/906, 510/175, 510/176

ABSTRACT:

In cleaning a substrate which has a metal material and a semiconductor material both exposed at the surface and which has been subjected to a chemical mechanical polishing treatment, the substrate is first cleaned with a first cleaning solution containing ammonia water, etc. and then with a second cleaning solution containing (a) a first complexing agent capable of easily forming a complex with the oxide of said metal material, etc. and (b) an anionic or cationic surfactant.

15 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 9

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

26. Document ID: US 6387821 B1

L3: Entry 26 of 37 File: USPT May 14, 2002

US-PAT-NO: 6387821
DOCUMENT-IDENTIFIER: US 6387821 B1

TITLE: Method of manufacturing a semiconductor device

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

h e b b cg b cc e

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aoki; Hidemitsu	Tokyo			JP

US-CL-CURRENT: 438/745; 257/E21.577, 257/E21.579, 438/747, 438/754

ABSTRACT:

In a method of manufacturing a semiconductor device having a multi-layer interconnection, after a via hole has been formed, the inside of the via hole is cleaned using a cleaning solution containing a complexing agent capable of forming a complex with contaminants of copper type metals.

10 Claims, 16 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 16

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

27. Document ID: US 6245650 B1

L3: Entry 27 of 37 File: USPT Jun 12, 2001

US-PAT-NO: 6245650
DOCUMENT-IDENTIFIER: US 6245650 B1

TITLE: Process for production of semiconductor device

DATE-ISSUED: June 12, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watanabe; Kaori	Tokyo			JP

US-CL-CURRENT: 438/580; 257/E21.011, 438/3

ABSTRACT:

A process for producing, starting from a silicon substrate, a semiconductor device having a capacitor part comprising platinum group metal electrodes and a ferroelectric film, which process comprises a cleaning step of cleaning and removing the platinum group metal-derived contaminants adhering onto (1) the silicon-based insulating film formed in contact with the platinum group metal of the electrode(s) and (2) the back surface of the silicon substrate, by using a cleaning solution comprising a chemical solution for metal removal and very small amounts of hydrofluoric acid and a chelating agent. This process can remove platinum group metal-derived contaminants reliably and can prevent the re-adhesion of the once-removed contaminants.

22 Claims, 18 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

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28. Document ID: US 6117775 A

L3: Entry 28 of 37 File: USPT Sep 12, 2000

US-PAT-NO: 6117775
DOCUMENT-IDENTIFIER: US 6117775 A
**** See image for Reexamination Certificate ****

TITLE: Polishing method

DATE-ISSUED: September 12, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kondo; Seiichi	Kokubunji			JP
Homma; Yoshio	Tokyo			JP
Sakuma; Noriyuki	Hachiouji			JP
Takeda; Kenichi	Tokorozawa			JP
Hinode; Kenji	Hachiouji			JP

US-CL-CURRENT: 438/690; 257/E21.304, 438/691, 438/692, 438/693, 438/745, 438/754

ABSTRACT:

A polishing technique wherein scratches, peeling, dishing and erosion are suppressed, a complex cleaning process and slurry supply/processing equipment are not required, and the cost of consumable items, such as slurries and polishing pads, is reduced. A metal film formed on an insulating film having a groove is polished with a polishing solution containing an oxidizer and a substance which renders oxides water-soluble, but not containing a polishing abrasive.

50 Claims, 41 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. De

29. Document ID: US 6060175 A

L3: Entry 29 of 37 File: USPT May 9, 2000

US-PAT-NO: 6060175
DOCUMENT-IDENTIFIER: US 6060175 A
**** See image for Certificate of Correction ****

TITLE: Metal-film laminate resistant to delamination

DATE-ISSUED: May 9, 2000

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INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swisher; Richard L.	Northfield	MN		

US-CL-CURRENT: 428/612; 428/623, 428/626, 428/675

ABSTRACT:

A flexible metal-film laminate can comprise a layered film structure having a metal layer securely bonded to a film layer. The laminate contains a unique metal-oxide attachment structure between the film and metal layer comprising randomly distributed regions of metal-oxide. After the metal/metal-oxide layer, a chromium metal or chromium alloy layer is formed before subsequent layers of copper, gold, etc. The peel strength of such a laminate is significantly improved over prior laminates and is resistant to peel strength reduction due to environmental stress. The preferred metal-film laminates made with polyester or polyimide can be used in the manufacture of high-quality, low cost, flexible printed circuit boards.

20 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

☐ 30. Document ID: US 5705443 A

L3: Entry 30 of 37 File: USPT Jan 6, 1998

US-PAT-NO: 5705443
DOCUMENT-IDENTIFIER: US 5705443 A

TITLE: Etching method for refractory materials

DATE-ISSUED: January 6, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stauf; Gregory	New Milford	CT		
Gardiner; Robin A.	Bethel	CT		
Kirlin; Peter S.	Bethel	CT		
Van Buskirk; Peter C.	Newtown	CT		

US-CL-CURRENT: 438/722; 204/192.35, 216/67, 216/75, 216/76, 257/E21.252, 257/E21.311, 438/710, 438/714, 438/720, 438/731

ABSTRACT:

A plasma-assisted dry etching process for etching of a metal containing material layer on a substrate to remove the metal containing material from the substrate, comprising (i) plasma etching the metal containing material and, (ii) contemporaneously with said plasma etching, contacting the metal containing material with an etch enhancing reactant in a sufficient amount and at a sufficient

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rate to enhance the etching removal of the metal containing material, in relation to a corresponding plasma etching of the metal containing material layer on the substrate in the absence of the etch enhancing reactant metal material being contacted with the etch enhancing reactant.

26 Claims, 15 Drawing figures
Exemplary Claim Number: 23
Number of Drawing Sheets: 8

Term	Documents
TREATMENT	1812453
TREATMENTS	209574
CHAMBER	1848118
CHAMBERS	517795
CVD	121465
CVDS	77
PROCESS	4742195
PROCESSES	1353030
CARBOXYLIC	416318
CARBOXYLICS	82
ACID	2257030
(((TREATMENT CHAMBER) OR CVD OR (PROCESS CHAMBER)) AND (CARBOXYLIC ACID) AND (REMOVING METAL)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	37

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Previous Page Next Page Go to Doc#

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☐ 31. Document ID: US 5480730 A

L3: Entry 31 of 37 File: USPT Jan 2, 1996

US-PAT-NO: 5480730
DOCUMENT-IDENTIFIER: US 5480730 A

TITLE: Metal-film laminate resistant to delamination

DATE-ISSUED: January 2, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swisher; Richard L.	Northfield	MN		

US-CL-CURRENT: 428/621; 428/623, 428/626, 428/675

ABSTRACT:

A flexible metal-film laminate can comprise a layered film structure having a metal layer securely bonded to a film layer. The laminate contains a unique metal-oxide attachment structure between the film and metal layer comprising randomly distributed regions of metal-oxide. The peel strength of such a laminate is significantly improved over prior laminates and is resistant to peel strength reduction due to environmental stress. The preferred metal-film laminates made with polyester or polyimide can be used in the manufacture of high-quality, low cost, flexible printed circuit boards.

45 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 32. Document ID: US 5364707 A

L3: Entry 32 of 37 File: USPT Nov 15, 1994

US-PAT-NO: 5364707
DOCUMENT-IDENTIFIER: US 5364707 A

TITLE: Metal-film laminate resistant to delamination

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DATE-ISSUED: November 15, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swisher; Richard L.	Northfield	MN		

US-CL-CURRENT: 428/612; 428/623, 428/626, 428/675

ABSTRACT:

A flexible metal-film laminate can comprise a layered film structure having a metal layer securely bonded to a film layer. The laminate contains a unique metal-oxide attachment structure between the film and metal layer comprising randomly distributed regions of metal-oxide. The peel strength of such a laminate is significantly improved over prior laminates and is resistant to peel strength reduction due to environmental stress. The preferred metal-film laminates made with polyester or polyimide can be used in the manufacture of high-quality, low cost, flexible printed circuit boards.

17 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

33. Document ID: US 5250105 A

L3: Entry 33 of 37 File: USPT Oct 5, 1993

US-PAT-NO: 5250105
DOCUMENT-IDENTIFIER: US 5250105 A

TITLE: Selective process for printing circuit board manufacturing

DATE-ISSUED: October 5, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gomes; Jose M. G.	Loures			PT
Rodrigues; Ana P. T. L.	Almada			PT

US-CL-CURRENT: 106/1.11; 106/1.28, 502/328, 502/330

ABSTRACT:

A new family of palladium based metallization catalyst compositions is diosed.

These catalysts are used in a process for the selective deposition of a metal on a substrate when a metallization mask (i.e. a plating resist) is used over the substrate.

Processes and compositions are also disclosed for manufacturing printed circuit boards, by using two metallization sequences, or one alone the latter comprising a

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so-called "selective process."

The process and composition are generally employed for the electroless plating of substrates, namely the metallization of plastics, ceramics, anodized aluminum and other materials.

4 Claims, 0 Drawing figures
Exemplary Claim Number: 1

34. Document ID: US 5213622 A

L3: Entry 34 of 37 File: USPT May 25, 1993

US-PAT-NO: 5213622
DOCUMENT-IDENTIFIER: US 5213622 A

TITLE: Cleaning agents for fabricating integrated circuits and a process for using the same

DATE-ISSUED: May 25, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bohling; David A.	Emmaus	PA		
Ivankovits; John C.	Allentown	PA		
Roberts; David A.	Carlsbad	CA		

US-CL-CURRENT: 134/3; 134/41, 257/E21.225, 257/E21.226, 257/E21.241, 510/175, 510/488

ABSTRACT:

This invention is a vapor-phase process for cleaning metal-containing contaminants from the surfaces of integrated circuits and semiconductors between the numerous fabricating steps required to manufacture the finished electronic devices. The process comprises contacting the surface to be cleaned with an effective amount of a cleaning agent comprising a carboxylic acid selected from acetic acid or formic acid at a temperature sufficient to form volatile metal-ligand complexes on the surface of the substrate to be cleaned. The volatile metal-ligand complexes are sublimed from the surface of the substrate providing a clean, substantially residue-free surface.

7 Claims, 1 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

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☐ 35. Document ID: US 5213621 A

L3: Entry 35 of 37 File: USPT May 25, 1993

US-PAT-NO: 5213621
DOCUMENT-IDENTIFIER: US 5213621 A

TITLE: Halogenated carboxylic acid cleaning agents for fabricating integrated circuits and a process for using the same

DATE-ISSUED: May 25, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ivankovits; John C.	Allentown	PA		
Bohling; David A.	Emmaus	PA		
Roberts; David A.	Carlsbad	CA		

US-CL-CURRENT: 134/3; 134/41, 257/E21.226, 257/E21.227, 257/E21.241, 510/175, 510/488

ABSTRACT:

This invention is a vapor-phase process for cleaning metal-containing contaminants from the surfaces of integrated circuits and semiconductors between the numerous fabricating steps required to manufacture the finished electronic devices. The process employs cleaning agents comprising an effective amount of a partially halogenated or fully halogenated linear or branched carboxylic acid having from 2 to about 10 carbon atoms wherein the halogen is selected from fluorine or chlorine. The process comprises contacting the surface to be cleaned with an effective amount of the desired cleaning agent at a temperature sufficient to form volatile metal-ligand complexes on the surface of the substrate to be cleaned. The volatile metal-ligand complexes are sublimed from the surfaces of the substrate providing a clean, substantially residue-free surface.

21 Claims, 1 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

☐ 36. Document ID: US 5137791 A

L3: Entry 36 of 37 File: USPT Aug 11, 1992

US-PAT-NO: 5137791
DOCUMENT-IDENTIFIER: US 5137791 A

TITLE: Metal-film laminate resistant to delamination

DATE-ISSUED: August 11, 1992

INVENTOR-INFORMATION:

h e b b cg b cc e

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swisher; Richard L.	Northfield	MN		

US-CL-CURRENT: 428/612; 428/623, 428/626, 428/632, 428/675, 428/938

ABSTRACT:

A flexible metal-film laminate can comprise a layered film structure having a metal layer securely bonded to a film layer. The laminate contains a unique metal-oxide attachment structure between the film and metal layer comprising randomly distributed regions of metal-oxide. The peel strength of such a laminate is significantly improved over prior laminates and is resistant to peel strength reduction due to environmental stress. The preferred metal-film laminates made with polyester or polyimide can be used in the manufacture of high-quality, low cost, flexible printed circuit boards.

29 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

☐ 37. Document ID: US 5112462 A

L3: Entry 37 of 37 File: USPT May 12, 1992

US-PAT-NO: 5112462
DOCUMENT-IDENTIFIER: US 5112462 A

TITLE: Method of making metal-film laminate resistant to delamination

DATE-ISSUED: May 12, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swisher; Richard L.	Northfield	MN		

US-CL-CURRENT: 205/165; 204/192.14, 204/298.24, 204/298.26, 205/924, 205/926, 427/250, 427/322, 427/537, 427/96, 428/609

ABSTRACT:

A flexible metal-film laminate can comprise a layered film structure having a metal layer securely bonded to a film layer. The laminate contains a unique metal-oxide attachment structure between the film and metal layer comprising randomly distributed regions of metal-oxide. The peel strength of such a laminate is significantly improved over prior laminates and is resistant to peel strength reduction due to environmental stress. The preferred metal-film laminates made with polyester or polyimide can be used in the manufacture of high-quality, low cost, flexible printed circuit boards.

30 Claims, 2 Drawing figures
Exemplary Claim Number: 8,10

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Number of Drawing Sheets: 2

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. De

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Term	Documents
TREATMENT	1812453
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(((TREATMENT CHAMBER) OR CVD OR (PROCESS CHAMBER)) AND (CARBOXYLIC ACID) AND (REMOVING METAL)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	37

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